**Mealy Machine:**

**Verilog Module:**

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 19:13:34 12/23/2022

// Design Name:

// Module Name: mealey

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module mealey(

output reg open,

input clock,

input reset,

input n,

input d

);

reg [1:0] state;

reg [1:0] nextstate;

reg nextopen;

parameter zero=0,five=1,ten=2;

parameter fifteen=3;

always @(n or d or state)

case(state)

zero:begin

if(n)begin

nextstate=five;

nextopen=0;

end

else if(d)begin

nextstate=ten;

nextopen=0;

end

else begin

nextstate=zero;

nextopen=0;

end

end

five:begin

if(n)begin

nextstate=ten;

nextopen=0;

end

else if(d)begin

nextstate=fifteen;

nextopen=1;

end

else begin

nextstate=five;

nextopen=0;

end

end

ten:begin

if(n)begin

nextstate=fifteen;

nextopen=1;

end

else if(d)begin

nextstate=fifteen;

nextopen=1;

end

else begin

nextstate=ten;

nextopen=0;

end

end

fifteen:begin

if(!reset)

nextstate=fifteen;

else

nextstate=0;

nextopen=1;

end

endcase

always @(posedge clock)

if(reset || (!n&&!d)) begin

state <= zero;

open <= 0;

end

else begin

state <= nextstate;

open <= nextopen;

end

endmodule

**TEXT FIXTURE:**

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 19:16:49 12/23/2022

// Design Name: mealey

// Module Name: F:/ISE PROJECTS/mealey/mealeytf.v

// Project Name: mealey

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: mealey

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module mealeytf;

// Inputs

reg clock;

reg reset;

reg n;

reg d;

// Outputs

wire open;

// Instantiate the Unit Under Test (UUT)

mealey uut (

.open(open),

.clock(clock),

.reset(reset),

.n(n),

.d(d)

);

parameter PERIOD = 100;

always begin

clock = 1;

#(PERIOD/2);

clock=0;

#(PERIOD/2);

end

initial begin

// Initialize Inputs

reset = 1;

n = 0;

d = 0;

#100;

reset = 0;

n = 1;

d = 0;

#100;

n = 0;

d = 1;

#100;

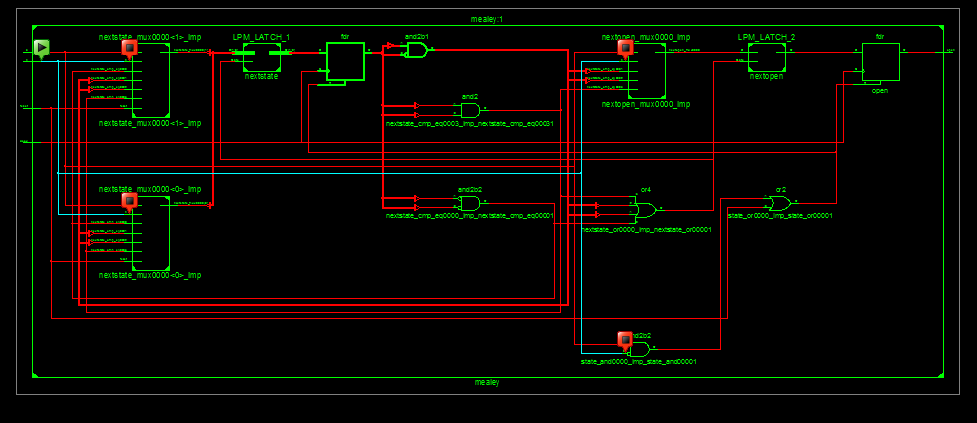
n = 0;

d = 0;

#100;

end

endmodule

**SCHEMATIC:**

**WaveForm:**

